

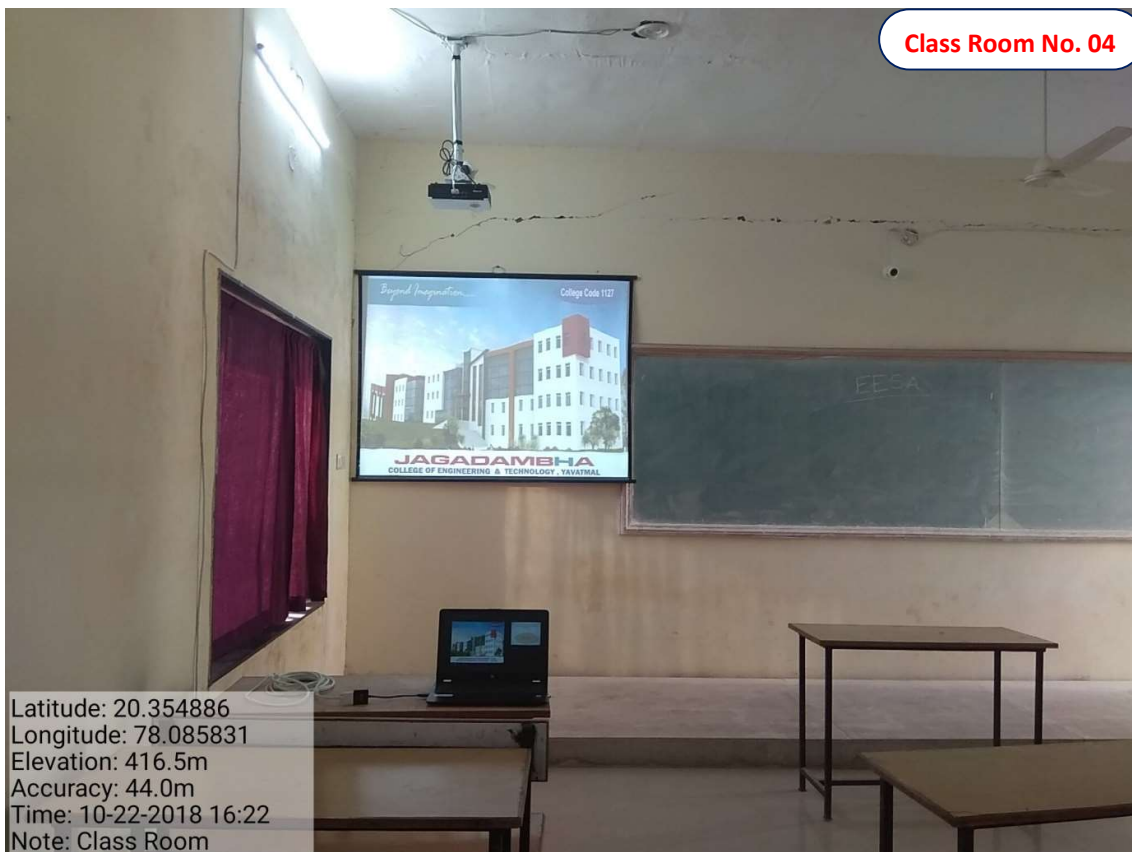


Photograph of the class rooms with ICT facilities



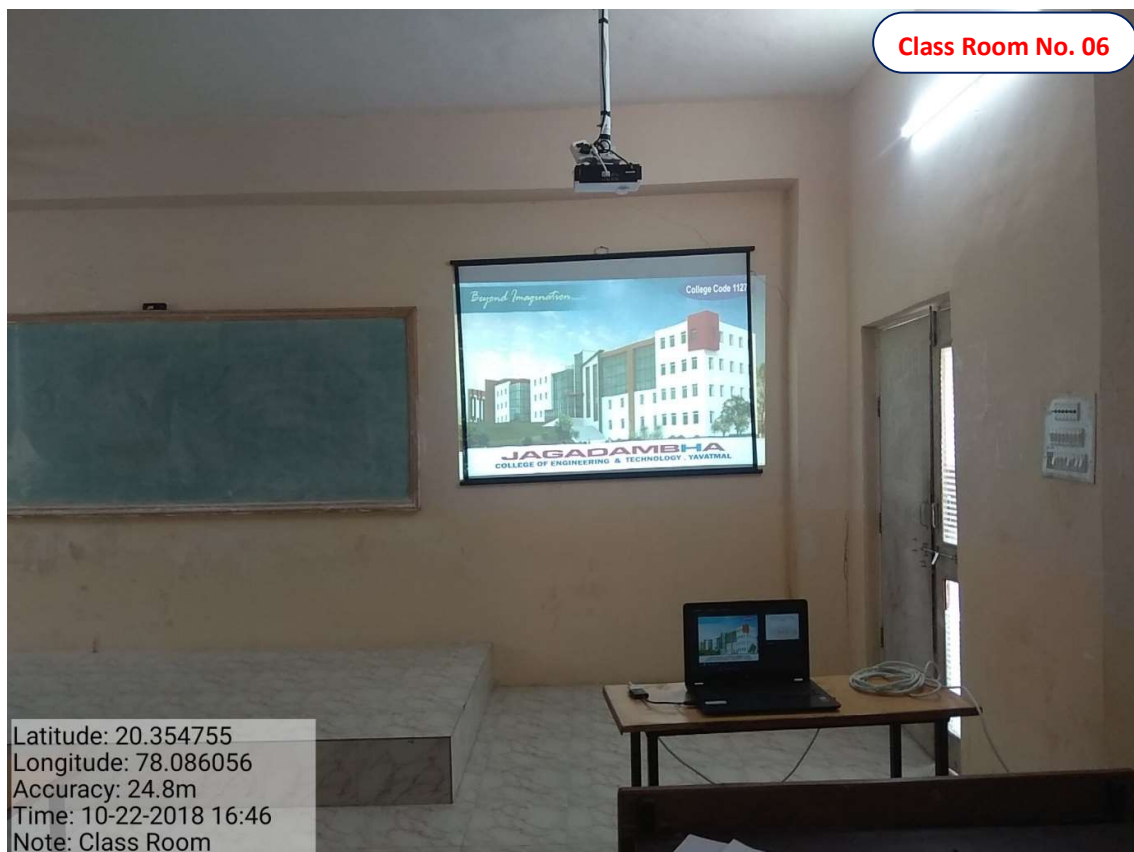


Photograph of the class rooms with ICT facilities



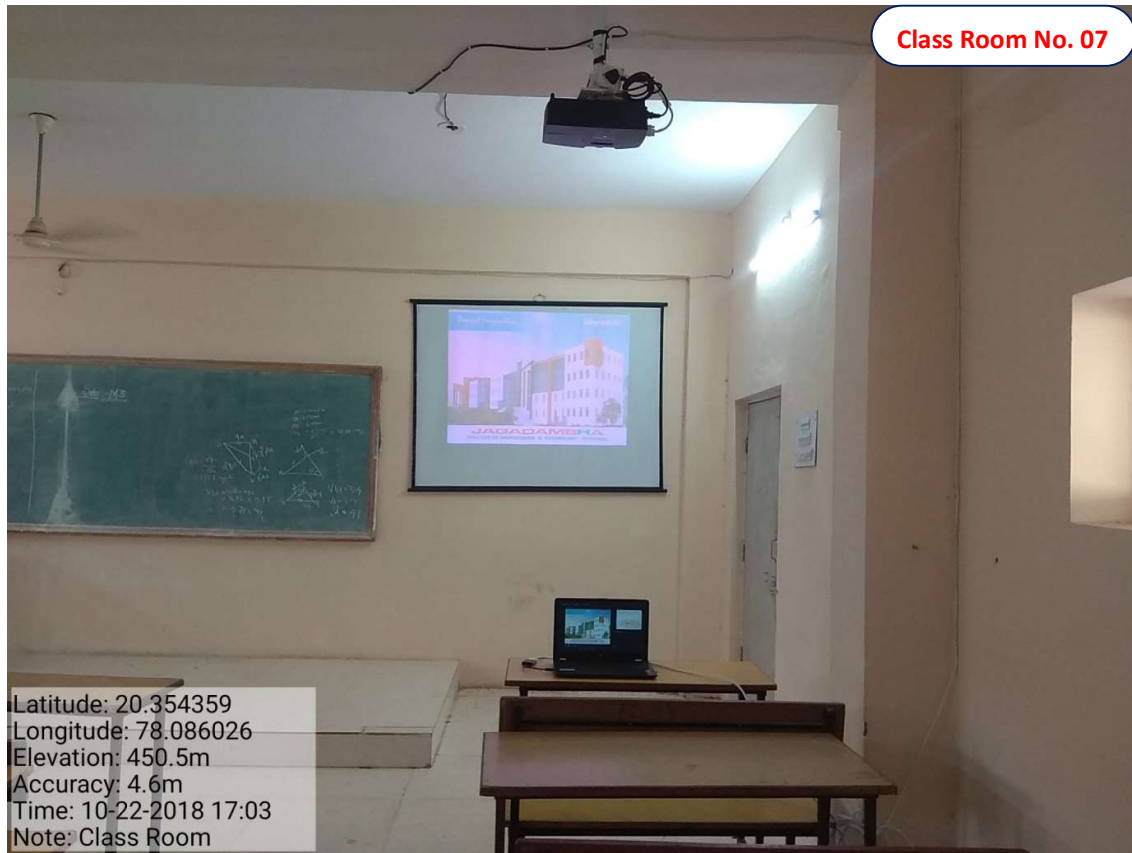


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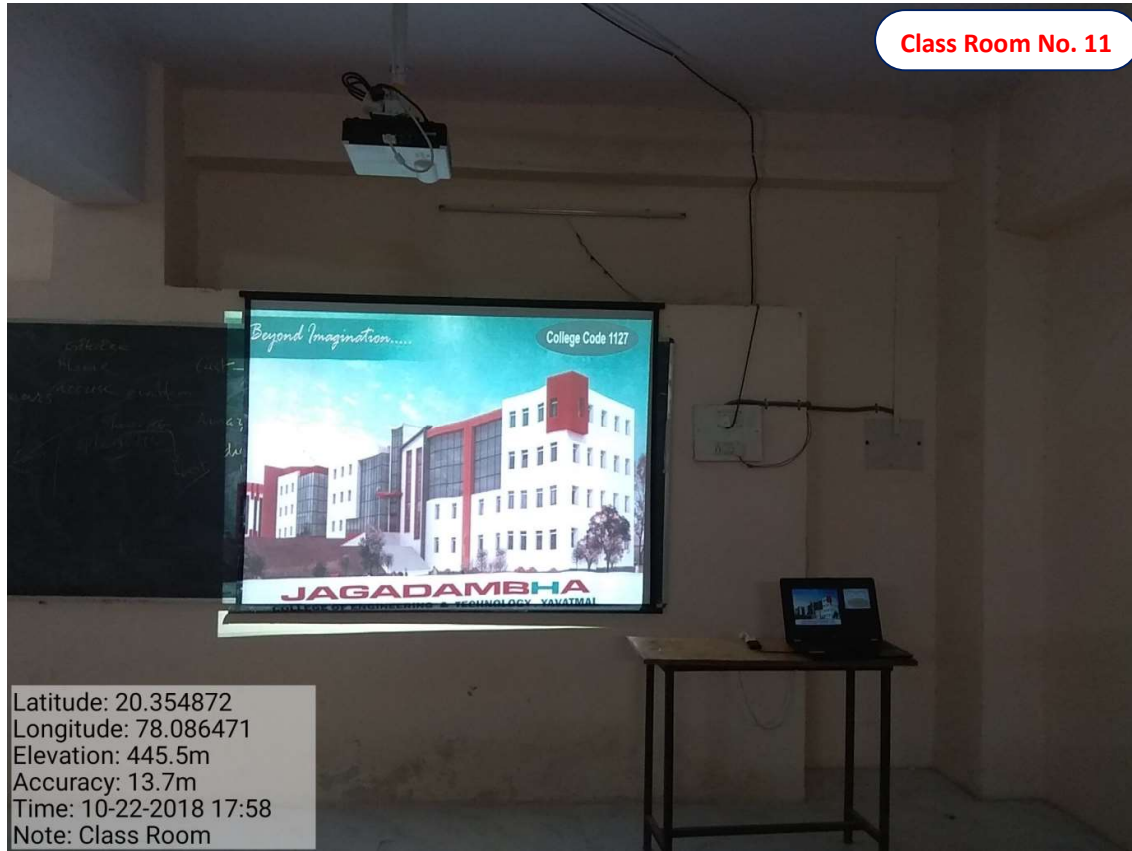


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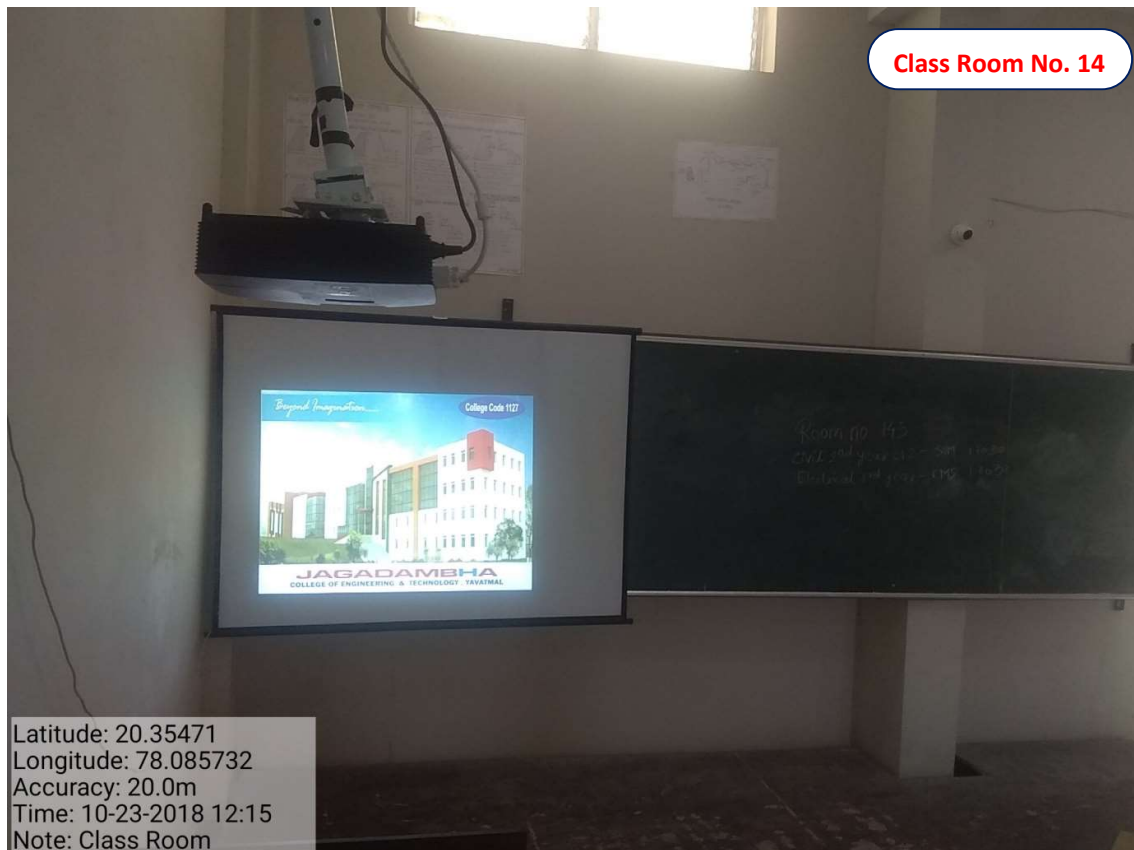
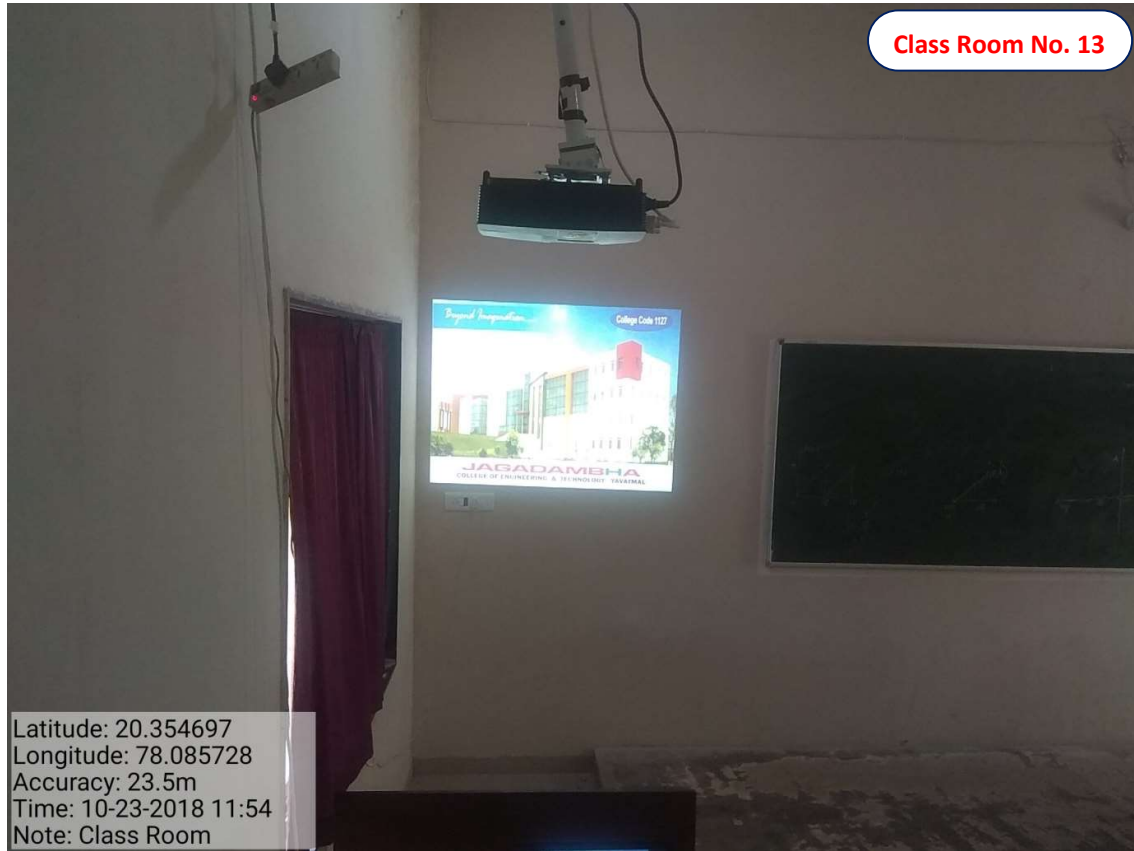


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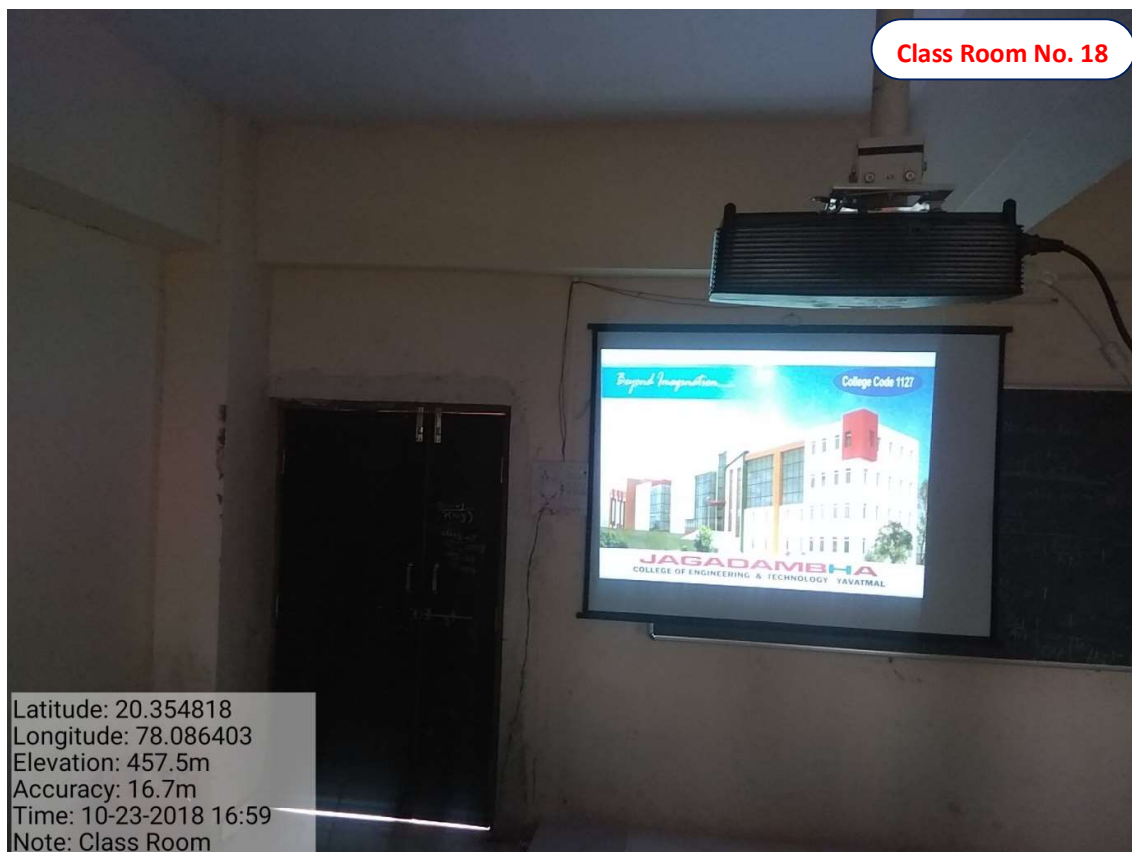


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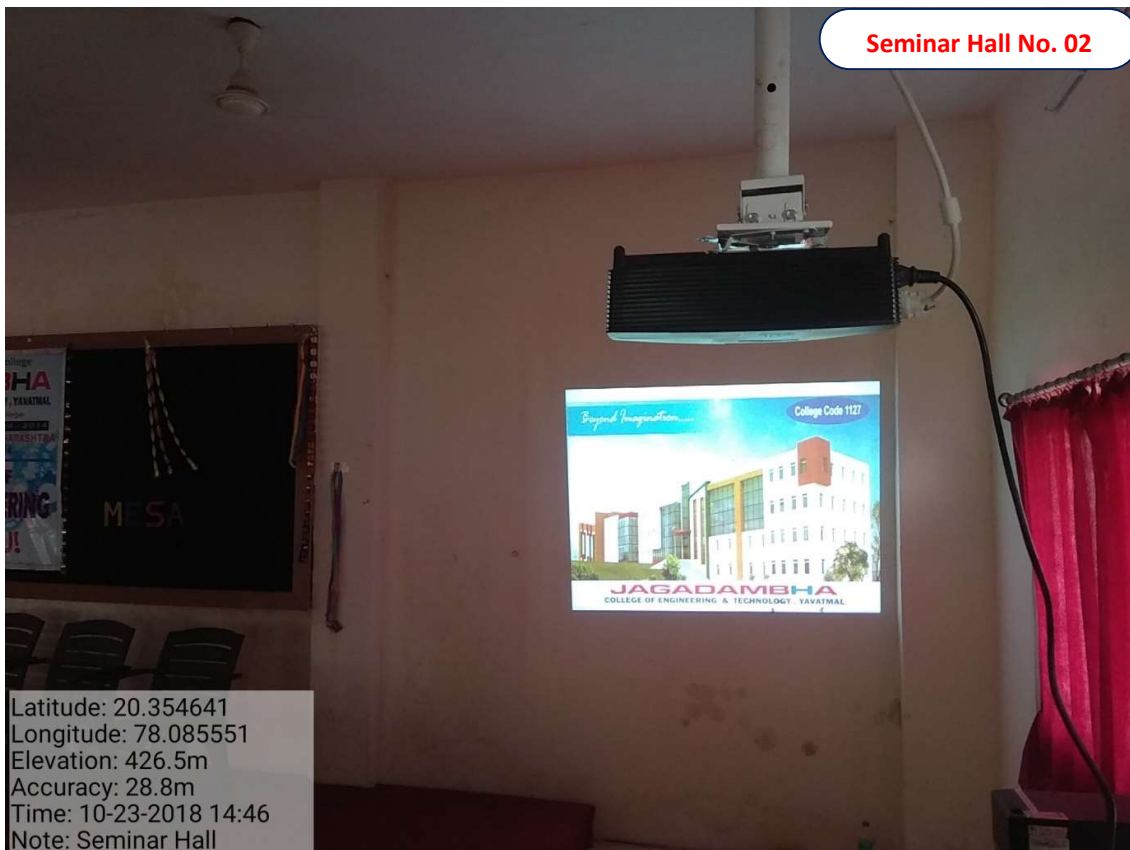


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COLLEGE OF ENGINEERING & TECHNOLOGY, YAVATMAL

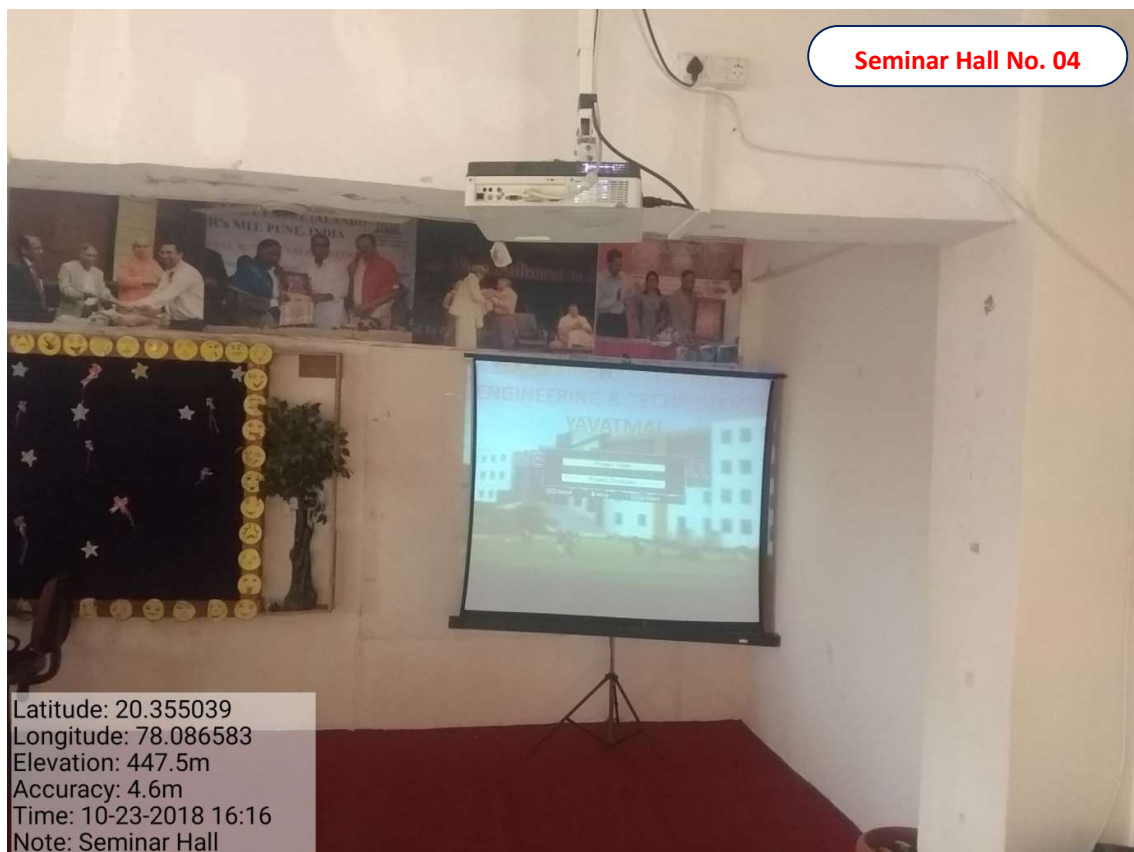
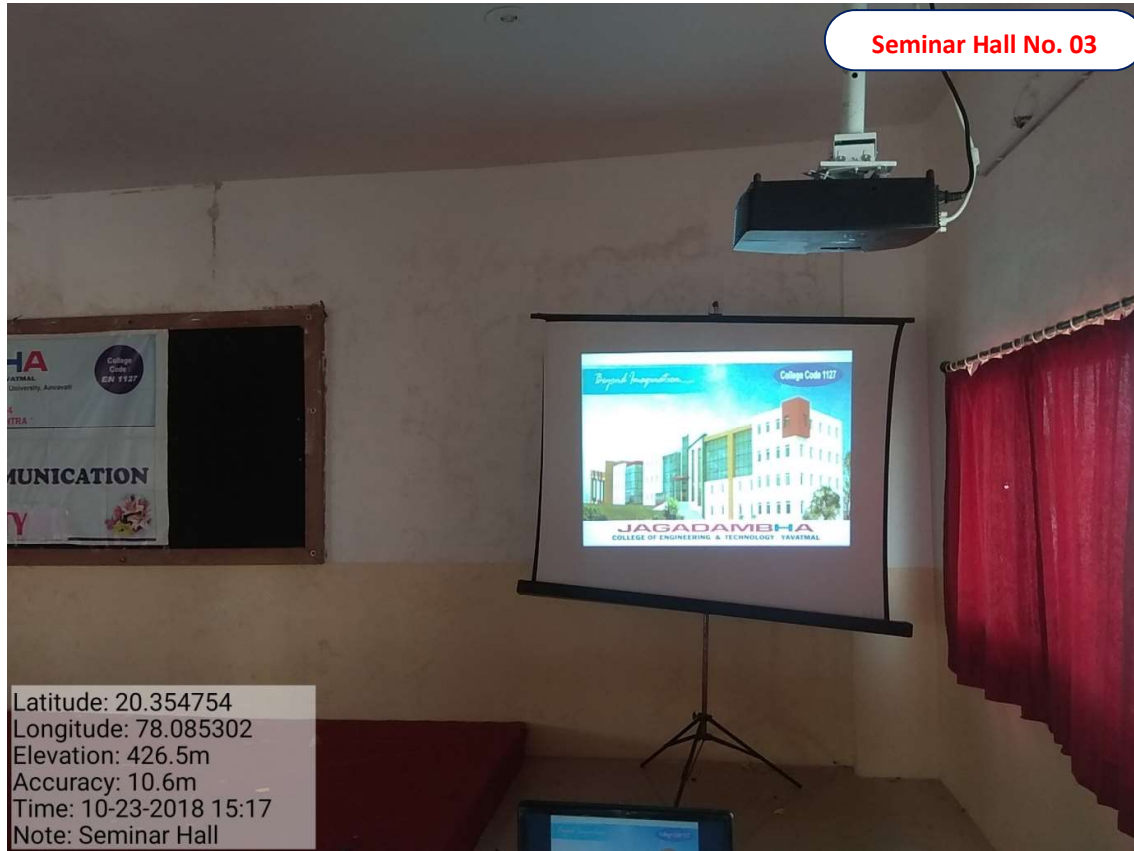


Photograph of the seminar halls with ICT facilities





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8251 USART

By Prof. K. L. Thakur
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 JAGADAMBHA COLLEGE OF ENGINEERING TECHNOLOGY, YAVATMAL

8251

- The 8251A is a programmable serial communication interface chip designed for synchronous and asynchronous serial data communication.
- It supports the serial transmission of data.
- It is packed in a 28 pin DIP.

Pin details

Pin	Description
1	Pin 1
2	Pin 2
3	Pin 3
4	Pin 4
5	Pin 5
6	Pin 6
7	Pin 7
8	Pin 8
9	Pin 9
10	Pin 10
11	Pin 11
12	Pin 12
13	Pin 13
14	Pin 14
15	Pin 15
16	Pin 16
17	Pin 17
18	Pin 18
19	Pin 19
20	Pin 20
21	Pin 21
22	Pin 22
23	Pin 23
24	Pin 24
25	Pin 25
26	Pin 26
27	Pin 27
28	Pin 28

Architecture

Arch - details

- The functional block diagram of 8251A consists five sections. They are:
 - Read/Write control logic
 - Transmitter
 - Receiver
 - Data bus buffer
 - Modem control.

Read/Write control logic

- The Read/Write Control logic interfaces the 8251A with CPU, determines the functions of the 8251A according to the control word written into its control register.
- It monitors the data flow.
- This section has three registers and they are control register, status register and data buffer.
- The active low signals RD, WR, CS and C/D (Low) are used for read/write operations with these three registers.

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Modem control

- The data lines D0 - D7 are connected to D0 - D7 of the processor to achieve parallel data transfer.
- The RESET and clock signals are supplied by the processor. Here the processor clock is directly connected to 8251A. This clock controls the parallel data transfer between the processor and 8251A.
- The output clock signal of 8085 is divided by suitable clock dividers like programmable timer 8254 and then used as clock for serial transmission and reception.

Modem control

- The TTL logic levels of the serial data lines and the control signals necessary for serial transmission and reception are converted to RS232C logic levels using MAX232 and then terminated on a standard 9-pin D-type connector.
- In 8251A the transmission and reception baud rates can be different or same.
- The device which requires serial communication with processor can be connected to this 9-pin D-type connector using 9-core cable
- The signals TxEMPTY, TxRDY and RxRDY can be used as interrupt signals to initiate interrupt driven data transfer scheme between processor and 8251.

Modem control

- The CPU reads the parallel data from the buffer register.
- When the input register loads a parallel data to buffer register, the RxRDY line goes high.
- The clock signal RxC (low) controls the rate at which bits are received by the USART.
- During asynchronous mode the signal SYNDET/BRKDET will indicate the break in the data transmission.
- During synchronous mode the signal SYNDET/BRKDET will indicate the reception of synchronous character.

8251 mode register

Bit	7	6	5	4	3	2	1	0
Number of Stop bits	0: 1 bit	1: 2 bits	2: 1.5 bits	3: 2 bits	4: 1.5 bits	5: 2 bits	6: 1.5 bits	7: 2 bits
Parity enable	0: disable	1: enable						
Character length	0: 5 bits	1: 6 bits	2: 7 bits	3: 8 bits	4: 9 bits	5: 10 bits	6: 11 bits	7: 12 bits

8251 command register

Bit	7	6	5	4	3	2	1	0
TE	transmit enable							
DTR	data terminal ready							
RE	receiver enable							
SEPRK	send break character							
ER	error reset							
RTS	request to send							
IR	internal reset							
ER	enter reset mode							

8251 status register

Bit	7	6	5	4	3	2	1	0
TxDY	transmit ready							
RxDY	receiver ready							
TxEMPTY	transmitter empty							
PE	parity error							
OE	overflow error							
FE	framing error							
SYNDET	sync character detected							
DSR	data set ready							



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8251 mode register

7	6	5	4	3	2	1	0
Number of Stop bits		Parity enable		Character length		Baud Rate	
00: 1 bit	0: disable	00: 5 bits	00: 5 baud	01: 6 bits	01: 6 baud	10: 7 bits	10: 7 baud
01: 1.5 bit	1: enable	10: 8 bits	10: 8 baud	11: 8 bits	11: 8 baud	11: 8 bits	11: 8 baud
10: 1.5 bit							
11: 2 bit							

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8251 command register

EH	IR	RTS	ER	ERR	RxIE	DTR	TxIE
----	----	-----	----	-----	------	-----	------

TxIE: transmit enable
 DTR: data terminal ready
 RxIE: receiver enable
 SBPK: send break character
 ER: error reset
 RTS: request to send
 IR: internal reset
 EH: enter burst mode

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8251 status register

DR	SYNDET	FE	OE	PE	TxRDY	RxRDY	TxEMPTY
----	--------	----	----	----	-------	-------	---------

TxRDY: transmit ready
 RxRDY: receiver ready
 TxEMPTY: transmitter empty
 PE: parity error
 OE: overrun error
 FE: framing error
 SYNDET: sync character detected
 DR: data set ready

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